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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/694,433	10/23/2000	Andrew Read	TRANS59	3072

7590 12/14/2005

WAGNER, MURABITO & HAO LLP
TWO NORTH MARKET STREET
THIRD FLOOR
SAN JOSE, CA 95113

EXAMINER	
CAO, CHUN	
ART UNIT	**PAPER NUMBER**
2115	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/694,433	READ ET AL.	
	Examiner	Art Unit	
	Chun Cao	2115	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *19-37* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-18* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAIL ACTION

1. Claims 1-37 are presented for examination. Claims 19-37 are newly added claims and presented for examination.

2. The text of those applicable section of Title 35, U.S. Code not included in this action can be found in the prior Office Action.

3. Applicant's response for the finality of rejection of the last office action is persuasive, therefore the finality of that action is hereby withdrawn, and the prosecution on the merit is hereby reopened.

Election/Restrictions

4. Newly submitted claims 19-37 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons:
Original claims 1-18, drawn to: reducing power utilized by a processor, and reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable, classified in class 713, subclass 322.
Newly added claims 19-37, drawn to: a computer system has a first transition time and second transition for transitioning from sleep voltage to an operating voltage, wherein the first transition time is greater than an allowed time, classified in class 713, subclass 310.

a. These inventions have acquired a separate status in the art as shown by their different classification;

b. The search required for one Group is not required for the other Groups for the reasons above restriction for examination purpose as indicated is proper.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 19-37 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

5. Claims 1-3, 5-11 and 13 are rejected under 35 U.S.C. 102(e) as being anticipated by Pole, II et al. (Pole), US patent no. 6,675,304.

Pole is a prior art reference cited in prior office action in IDS paper no. 20040917.

As per claim 1, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40], wherein said value of the core voltage is not sufficient to maintain processing activity in said processor [deep sleep state, col. 1, line 30-34].

As per claim 2, Pole teaches of determining the processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled comprises monitoring a stop clock signal [col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 3, Pole teaches of reducing core voltage to the processor to a value sufficient to maintain state during the state in which system clock is disabled [col. 1, lines 30-34] comprises: furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67].

As per claim 5, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16];

reducing core voltage to the processor to a value sufficient to maintain state during the mode of which system clock is disable [col. 4, lines 15-40]; and

transferring operation of a voltage regulator furnishing core voltage in a mode in which power is dissipated during reductions in core voltage to a mode in which power is saved during a voltage transition when it is determined at a processor is transitioning from a computing mode to a mode is which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 6, Pole teaches of returning the voltage regulator to its original mode of operation when the value of the core voltage sufficient to maintain state during the mode in which system clock is disabled is reached [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

6. As per claim 7, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11], wherein the level less than that for operating the processor in a computing mode is sufficient to maintain state of the processor [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

As per claim 8, Pole discloses that the voltage regulator comprises means for accepting binary signals [LO/HI signals] indicating different voltage level [fig. 2; col. 3, lines 43-61; "A signal VR_LO/HI#...adjust the voltage level supplied by the voltage regulator 52 up or down"].

As per claim 9, Pole discloses that the voltage regulator comprises:

Selection circuitry, means for furnishing a plurality of signals at the input to the selection circuitry and means for controlling the selection by the selection circuitry [fig. 2; col. 3, lines 31-67].

As per claim 10, Pole discloses a multiplexor and means for controlling the selection by the selection circuitry including a control terminal for receiving signals indicating a system clock to the processor is being terminated [fig. 2; col. 3, lines 31-67].

7. As per claim 11, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11], means for reducing the selectable voltage below a lowest level the voltage regulator is specified to output [col. 1, lines 30-34; col. 4, lines 15-40; col. 5, lines 10-16].

8. As per claim 13, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

circuitry for conserving charge [battery 60] stored by the voltage regulator when the selectable voltage decreases; and means for enabling the circuitry for conserving charge stored by the voltage regulator when the selectable voltage decreases [col. 3, lines 43-67; col. 4, lines 15-40; col. 5, lines 10-16].

9. Claims 4, 12 and 14-18 are rejected under 35 U.S.C. 103 (a) as being unpatentable over Pole, II et al. (Pole), US patent no. 6,675,304 in view of Applicant Admitted Prior Art (AAPA) and "High-speed, Digitally adjusted step-down controllers for notebook CPUs" Maxim, July 2000, pages 1-28 (hereinafter "Maxim).

As per claim 4, Pole teaches a method for reducing power utilized by a processor [fig. 5] comprising the steps of:

determining that a processor is transitioning from a computing mode to a mode in which system clock to the processor is disabled [col. 1, lines 30-34; col. 4, lines 15-32; col. 5, lines 10-16]; and

reducing core voltage to the processor to a value sufficient to maintain state during the mode in which system clock is disable [col. 4, lines 15-40] by:

furnishing an input to reduce an output voltage provided by a voltage regulator furnishing core voltage to the processor [col. 3, lines 31-67]; and

providing a control signal to the voltage regulator to reduce its output voltage below a specified output voltage [col. 4, lines 5-7].

Pole does not explicitly teach of providing a feedback to the voltage regulator.

AAPA teaches of providing a feedback to the voltage regulator [Maxim 1711, page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller, wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Pole and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 18, Pole teaches that the output voltage to which said voltage regulator is reduced depends upon output voltage of said voltage regulator prior to

furnishing the input to reduce the output voltage provided by the voltage regulator [col. 3, lines 43-67].

10. As per claim 12, Pole discloses a circuit [fig. 2] for providing a regulated voltage to a processor comprising:

a voltage regulator [52, figures 1, 2] having: an output terminal [col. 3, lines 31-55; " the output from the voltage regulator 52", inherently, there is an output terminal in the voltage regulator 52] providing a selectable voltage [col. 3, lines 43-50, "...adjust the voltage level supplied by the voltage regulator 52 up or down" and "to indicate that the voltage level from the voltage regulator 52 is changing"];

input terminal [fig. 2] for receiving signals indicating the selectable voltage level [col. 3, lines 31-55];

means for providing signal at the input terminal of the voltage regulator for selecting a voltage for operating the processor in a computing mode and a voltage of a level less than that for operating the processor in computing mode [col. 4, lines 2-11],

means for reducing the selectable voltage below a level provided by the voltage regulator [col. 4, lines 2-11].

Pole does not explicitly disclose a voltage regulator feedback circuit and a voltage divider network.

AAPA discloses a voltage regulator including a voltage regulator feedback circuit and a voltage divider network [page 10, lines 6-9].

Furthermore, Maxim teaches a Maxim 1711 is a step-down controller with a voltage divider network [see page 1], wherein Maxim 1711 is implemented in a computer system to reduce voltage level to a CPU core [see page 1].

It would have been obvious to one of ordinary skill in the art at time the invention to combine the teachings of Orton and AAPA because the specify teachings of AAPA stated above would allow the processor to run stable and reliable by adjusting the core voltage accordingly.

As per claim 14 is contained same limitations as set forth in claim 12. Therefore, same rejection is applied.

As per claim 15, Pole teaches that the first voltage is for operating the processor in a computing mode and the second voltage is a level less than that for operating the processor in the computing mode [col. 4, lines 2-7].

As to claims 16 and 17, Maxim discloses that the feedback circuit comprises a voltage divider [see page 1].

Response to Arguments

11. Applicant's arguments filed on 11/28/05 have been fully considered but are moot in view of new ground(s) of rejection.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chun Cao whose telephone number is 571-272-3664. The examiner can normally be reached on Monday-Friday from 7:30 am-4:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas C. Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CHUN CAO
PRIMARY EXAMINER

Dec 9, 2005